Amendments to the Claims

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

Listing of the Claims

Claims 1-10 (canceled)

11. (previously presented) A method of fabricating a chip package comprising the steps of:

separating a wafer into multiple dies;

after said separating said wafer, joining one of said multiple dies and a substrate, wherein an opening in said substrate exposes said one of said multiple dies;

depositing a tin-containing ball into said opening in said substrate; and

after said joining said one of said multiple dies and said substrate, separating said substrate into multiple portions.

12. (previously presented) The method of claim 11, wherein said one of said multiple dies comprises a semiconductor substrate, multiple integrated circuit devices on said semiconductor substrate, multiple pads, multi-level underlying metal layers under said multiple pads, multiple insulating dielectric layers intervening said multi-level underlying metal layers, a passivation layer and an overlying metal layer, wherein said multiple pads are connected to said multiple integrated circuit devices through said multi-level underlying metal layers, wherein multiple

openings in said passivation layer are over said multiple pads and expose said multiple pads, wherein said overlying metal layer is on said multiple pads exposed by said multiple openings in said passivation layer, and wherein said opening in said substrate exposes said overlying metal layer in the step of said joining said one of said multiple dies and said substrate.

13. (previously presented) The method of claim 11, wherein said opening in said substrate is formed before said joining said one of said multiple dies and said substrate.

Claim 14 (canceled)

15. (previously presented) The method of claim 11, wherein said one of said multiple dies comprises a semiconductor substrate, multiple integrated circuit devices on said semiconductor substrate, multiple pads, multi-level underlying metal layers under said multiple pads, multiple insulating dielectric layers intervening said multi-level underlying metal layers, and a passivation layer, wherein said multiple pads are connected to said multiple integrated circuit devices through said multi-level underlying metal layers, wherein multiple openings in said passivation layer are over said multiple pads and expose said multiple pads, and wherein said opening in said substrate is over one of said multiple pads after said joining said one of said multiple dies and said substrate.

Claim 16 (canceled)

17. (previously presented) The method of claim 11, wherein said one of said multiple dies comprises a semiconductor substrate, multiple integrated circuit devices on said semiconductor substrate, multiple pads, multi-level underlying metal layers under said multiple pads, multiple insulating dielectric layers intervening said multi-level underlying metal layers, a passivation layer and an overlying metal layer, wherein said multiple pads are connected to said multiple integrated circuit devices through said multi-level underlying metal layers, wherein multiple openings in said passivation layer are over said multiple pads and expose said multiple pads, wherein said overlying metal layer is over said passivation layer, and wherein said opening in said substrate exposes said overlying metal layer in the step of said joining said one of said multiple dies and said substrate.

Claim 18 (canceled)

19. (previously presented) The method of claim 11 further comprising depositing an adhesive material on said substrate, followed by said joining said one of said multiple dies and said substrate using said adhesive material.

20. (previously presented) The method of claim 11, after said joining said one of said multiple dies and said substrate, further comprising encapsulating said one of said multiple dies with a molding material.

Claims 21 and 22 (canceled)

23. (previously presented) The method of claim 11, wherein said substrate comprises bismaleimide triazine (BT).

24. (previously presented) The method of claim 11, wherein said tin-containing ball comprises a tin-silver alloy.

25. (previously presented) The method of claim 11, wherein said opening in said substrate is formed using a process comprising mechanical drilling before said joining said one of said multiple dies and said substrate.

Claims 26-41 (canceled)

42. (currently amended) A method of fabricating a chip package comprising the steps of:

providing a first die, separated from a wafer, comprising a semiconductor substrate, multiple integrated circuit devices on said semiconductor substrate, multiple pads, multi-level underlying metal layers under said multiple pads, multiple insulating dielectric layers intervening said multi-level underlying metal layers, and a passivation layer, wherein said multiple pads are connected to said multiple integrated circuit devices through said multi-level underlying metal layers, and wherein multiple openings in said passivation layer are over said multiple pads and expose said multiple pads;

depositing an adhesive material on a substrate;

joining a first side of said first die and said substrate using said adhesive material, wherein a first opening in said substrate exposes said first side of said first die, wherein said first

opening in said substrate is over one of said multiple pads, and wherein said passivation layer is at said first side;

joining a first side of a second die and said substrate using said adhesive material, wherein a second opening in said substrate exposes said first side of said second die;

encapsulating a second side and sidewall of said first die, a second side and sidewall of said second die, and a gap between said first and second dies with a molding material, wherein said second side of said first die is opposite to said first side of said first die, and said second side of said second die is opposite to said first side of said second die, wherein said gap is filled completely with said molding material, and wherein said molding material has a surface with a first region over said gap and multiple second regions over said second side of said first die and over said second side of said second die, wherein said first region is at a same horizontal level as said multiple second regions; and

after said encapsulating said second side and sidewall of said first die, said second side and sidewall of said second die, and said gap between said first and second dies with said molding material, separating said molding material and said substrate into multiple portions to form said chip package, wherein said separating said molding material and said substrate comprises a sawing process.

43. (currently amended) The method of claim 42, wherein said first die further comprises an overlying metal layer on said multiple pads exposed by said multiple openings in said passivation layer, and ~~wherein~~ said first opening in said substrate exposes said overlying metal layer in the step of said joining said first side of said first die and said substrate.

44. (previously presented) The method of claim 42, after said encapsulating said second side and sidewall of said first die, said second side and sidewall of said second die, and said gap between said first and second dies with said molding material, further comprising forming a tin-containing ball connected to said first die through said first opening in said substrate, wherein said tin-containing ball comprises a tin-silver alloy.

45. (currently amended) The method of claim 42, wherein said first die further comprises an overlying metal layer over said passivation layer, and ~~wherein~~ said first opening in said substrate exposes said overlying metal layer in the step of said joining said first side of said first die and said substrate.

46. (previously presented) The method of claim 42, wherein said molding material comprises a polymer.

47. (previously presented) The method of claim 42, wherein said substrate has a thickness between 150 and 300 micrometers.

48. (previously presented) The method of claim 42, wherein said first opening is formed before said joining said first side of said first die and said substrate.

49. (previously presented) The method of claim 42, wherein said substrate comprises bismaleimide triazine (BT).

50. (previously presented) The method of claim 42, after said joining said first side of said first die and said substrate, further comprising forming a metal conductor through said first opening in said substrate.

51. (previously presented) The method of claim 42, after said encapsulating said second side and sidewall of said first die, said second side and sidewall of said second die, and said gap between said first and second dies with said molding material, further comprising forming a tin-containing ball connected to said first die through said first opening in said substrate.

52. (previously presented) A method of fabricating a chip package comprising the steps of:

providing a die, separated from a wafer, comprising a semiconductor substrate, multiple integrated circuit devices on said semiconductor substrate, multiple pads, multi-level underlying metal layers under said multiple pads, multiple insulating dielectric layers intervening said multi-level underlying metal layers, a passivation layer and a UBM layer, wherein said multiple pads are connected to said multiple integrated circuit devices through said multi-level underlying metal layers, wherein multiple openings in said passivation layer are over said multiple pads and expose said multiple pads, and wherein said UBM layer is on said multiple pads exposed by said multiple openings in said passivation layer;

joining said die and a substrate, wherein an opening in said substrate exposes said UBM layer; and

after said joining said die and said substrate, separating said substrate into multiple portions.

53. (previously presented) The method of claim 52, after said joining said die and said substrate, further comprising depositing a conductive material into said opening in said substrate.

54. (previously presented) The method of claim 53, wherein said conductive material comprises tin.

55. (previously presented) The method of claim 53, wherein said conductive material comprises a tin-silver alloy.

56. (previously presented) The method of claim 53, wherein said conductive material comprises a tin-lead alloy.

Claim 57 (canceled)

58. (previously presented) The method of claim 52, after said joining said die and said substrate, further comprising encapsulating said die with a molding material.

Claim 59 (canceled)

60. (previously presented) The method of claim 52 further comprising depositing an adhesive material on said substrate, followed by said joining said die and said substrate using said adhesive material.

61. (previously presented) The method of claim 52, wherein said opening in said substrate is formed before said joining said die and said substrate.

62. (previously presented) The method of claim 52, wherein said UBM layer comprises copper.

63. (previously presented) A method of fabricating a chip package comprising the steps of:

providing a die, separated from a wafer, comprising a semiconductor substrate, multiple integrated circuit devices on said semiconductor substrate, multiple pads, multi-level underlying metal layers under said multiple pads, multiple insulating dielectric layers intervening said multi-level underlying metal layers, a passivation layer and an overlying metal layer, wherein said multiple pads are connected to said multiple integrated circuit devices through said multi-level underlying metal layers, wherein multiple openings in said passivation layer are over said multiple pads and expose said multiple pads, and wherein said overlying metal layer is on said multiple pads;

joining said die and a substrate, wherein an opening in said substrate exposes said overlying metal layer of said die;

after said joining said die and said substrate, forming a metal conductor through said opening in said substrate; and

after said joining said die and said substrate, separating said substrate into multiple portions.

64. (previously presented) The method of claim 63, wherein said metal conductor comprises tin.

65. (previously presented) The method of claim 63, wherein said metal conductor comprises a tin-lead alloy.

66. (previously presented) The method of claim 63, wherein said metal conductor comprises a tin-silver alloy.

67. (previously presented) The method of claim 63, wherein said separating said substrate comprises a sawing process.

68. (previously presented) The method of claim 63, after said joining said die and said substrate, further comprising encapsulating said die with an epoxy-based resin.

69. (previously presented) The method of claim 63, wherein said joining said die and said substrate is performed under a pressure between 1.5 and 2.5 Megapascals (Mpa).

Claim 70 (canceled)

71. (previously presented) The method of claim 63, after said joining said die and said substrate, further comprising encapsulating said die with a molding material.

Claim 72 (canceled)

73. (previously presented) The method of claim 63 further comprising depositing an adhesive material on said substrate, followed by said joining said die and said substrate using said adhesive material.

74. (previously presented) The method of claim 63, wherein said opening in said substrate is formed before said joining said die and said substrate.

Claims 75-101 (canceled)

102. (previously presented) A method of fabricating a chip package comprising the steps of:

providing a die, separated from a wafer, comprising a semiconductor substrate, multiple integrated circuit devices on said semiconductor substrate, multiple pads, multi-level underlying metal layers under said multiple pads, multiple insulating dielectric layers intervening said multi-level underlying metal layers, a passivation layer and a UBM layer, wherein said multiple pads are connected to said multiple integrated circuit devices through said multi-level underlying metal layers, wherein multiple openings in said passivation layer are over said multiple pads and expose said multiple pads, and wherein said UBM layer is on said multiple pads exposed by said multiple openings in said passivation layer;

joining said die and a substrate, wherein an opening in said substrate exposes said UBM layer; and

depositing a conductive material into said opening in said substrate.

103. (previously presented) The method of claim 102, wherein said conductive material comprises tin.

104. (previously presented) The method of claim 102, wherein said conductive material comprises a tin-silver alloy.

105. (previously presented) The method of claim 102, wherein said conductive material comprises a tin-lead alloy.

106. (previously presented) The method of claim 102, after said depositing said conductive material, further comprising separating said substrate into multiple portions.

107. (previously presented) The method of claim 102, after said joining said die and said substrate, further comprising encapsulating said die with a molding material.

Claim 108 (canceled)

109. (previously presented) The method of claim 102 further comprising depositing an adhesive material on said substrate, followed by said joining said die and said substrate using said adhesive material.

110. (previously presented) The method of claim 102, wherein said opening in said substrate is formed before said joining said die and said substrate.

111. (previously presented) The method of claim 102, wherein said UBM layer comprises copper.

Claims 112-116 (Canceled)

117. (previously presented) A method of fabricating a chip package comprising the steps of:

providing a die, separated from a wafer, comprising a semiconductor substrate, multiple integrated circuit devices on said semiconductor substrate, multiple pads, multi-level underlying metal layers under said multiple pads, multiple insulating dielectric layers intervening said multi-level underlying metal layers, a passivation layer and an overlying metal layer, wherein said multiple pads are connected to said multiple integrated circuit devices through said multi-level underlying metal layers, wherein multiple openings in said passivation layer are over said multiple pads and expose said multiple pads, and wherein said overlying metal layer is over said passivation layer; and

joining said die and a substrate, wherein an opening in said substrate exposes said overlying metal layer.

118. (previously presented) The method of claim 117, wherein said opening in said substrate is formed before said joining said die and said substrate.

119. (previously presented) The method of claim 117, after said joining said die and said substrate, further comprising separating said substrate into multiple portions.

120. (previously presented) The method of claim 117, after said joining said die and said substrate, further comprising encapsulating said die with an epoxy-based resin.

121. (previously presented) The method of claim 117, after said joining said die and said substrate, further comprising encapsulating said die with a molding material.

Claim 122 (canceled)

123. (previously presented) The method of claim 117 further comprising depositing an adhesive material on said substrate, followed by said joining said die and said substrate using said adhesive material.

124. (previously presented) The method of claim 117, after said joining said die and said substrate, further comprising depositing a conductive material into said opening in said substrate.

125. (previously presented) The method of claim 124, wherein said conductive material comprises tin.

126. (previously presented) The method of claim 124, wherein said conductive material comprises a tin-silver alloy.

127. (previously presented) A method of fabricating a chip package comprising the steps of:

providing a die, separated from a wafer, comprising a semiconductor substrate, multiple integrated circuit devices on said semiconductor substrate, multiple pads, multi-level underlying metal layers under said multiple pads, multiple insulating dielectric layers intervening said multi-level underlying metal layers, and a passivation layer, wherein said multiple pads are connected to said multiple integrated circuit devices through said multi-level underlying metal layers, and wherein multiple openings in said passivation layer are over said multiple pads and expose said multiple pads;

depositing an adhesive material on a substrate;

joining a first side of said die and said substrate using said adhesive material, wherein an opening in said substrate exposes said first side of said die, and wherein said passivation layer is at said first side;

after said joining said first side of said die and said substrate, encapsulating a second side and sidewall of said die with a molding material, wherein said second side of said die is opposite to said first side of said die; and

after said encapsulating said second side and sidewall of said die with said molding material, separating said molding material and said substrate into multiple portions to form said chip package, wherein said separating said molding material and said substrate comprises a sawing process.

128. (previously presented) The method of claim 127, wherein said opening in said substrate is formed before said joining said first side of said die and said substrate.

129. (previously presented) The method of claim 127, wherein said molding material comprises a polymer.

Claims 130 and 131 (canceled)

132. (previously presented) The method of claim 127, after said joining said first side of said die and said substrate, further comprising forming a metal conductor through said opening in said substrate.

133. (previously presented) The method of claim 127, after said encapsulating said second side and sidewall of said die with said molding material, further comprising forming a tin-containing ball connected to said die through said opening in said substrate.

134. (currently amended) A method of fabricating a chip package comprising the steps of:

separating a wafer into multiple dies, wherein one of said multiple dies comprises a semiconductor substrate, multiple integrated circuit devices on said semiconductor substrate, multiple pads, multi-level underlying metal layers under said multiple pads, multiple insulating dielectric layers intervening said multi-level underlying metal layers, and a passivation layer, wherein said multiple pads are connected to said multiple integrated circuit devices through said multi-level underlying metal layers, and wherein multiple openings in said passivation layer are over said multiple pads and expose said multiple pads;

after said separating said wafer, joining a first side of said one of said multiple dies and a substrate, wherein an opening in said substrate exposes said first side of said one of said multiple dies, and wherein said passivation layer is at said first side;

after said joining said first side of said one of said multiple dies and said substrate, forming a metal conductor through said opening in said substrate;

after said joining said first side of said one of said multiple dies and said substrate, encapsulating a second side and sidewall of said one of said multiple dies with a molding material, wherein said first side of said one of said multiple dies is opposite to said second side of said one of said multiple dies; and

after said encapsulating said second side and sidewall of said one of said multiple dies with said molding material, separating said molding material and said substrate into multiple portions to form said chip package, wherein said separating said molding material and said substrate comprises a sawing process.

135. (currently amended) The method of claim 134, wherein said one of said multiple dies further comprises an overlying metal layer on said multiple pads exposed by said multiple openings in said passivation layer, and ~~wherein~~ said opening in said substrate exposes said overlying metal layer in the step of said joining said first side of said one of said multiple dies and said substrate.

136. (previously presented) The method of claim 134, wherein said opening in said substrate is formed before said joining said first side of said one of said multiple dies and said substrate.

137. (previously presented) The method of claim 134, wherein said metal conductor comprises a tin-lead alloy.

138. (previously presented) The method of claim 134, wherein said joining said first side of said one of said multiple dies and said substrate is performed under a pressure between 1.5 and 2.5 Megapascals (Mpa).

139. (previously presented) The method of claim 134 further comprising depositing an adhesive material on said substrate, followed by said joining said first side of said one of said multiple dies and said substrate using said adhesive material.

140. (previously presented) The method of claim 134, wherein said molding material comprises a polymer.

141. (previously presented) The method of claim 134, wherein said substrate has a thickness between 150 and 300 micrometers.

Claim 142 (canceled)

143. (previously presented) The method of claim 134, wherein said substrate comprises bismaleimide triazine (BT).

144. (previously presented) The method of claim 134, wherein said metal conductor comprises tin.

145. (previously presented) The method of claim 134, wherein said opening in said substrate is formed using a process comprising mechanical drilling before said joining said first side of said one of said multiple dies and said substrate.

146. (previously presented) The method of claim 11, wherein said opening in said substrate is formed using a process comprising laser drilling before said joining said one of said multiple dies and said substrate.

147. (previously presented) The method of claim 11, wherein said substrate has a thickness between 150 and 300 micrometers.

148. (previously presented) The method of claim 12, wherein said overlying metal layer comprises copper.

149. (previously presented) The method of claim 12, wherein said overlying metal layer comprises nickel.

Claim 150 (canceled)

151. (previously presented) The method of claim 42, wherein said first opening in said substrate is formed using a process comprising laser drilling before said joining said first side of said first die and said substrate.

152. (previously presented) The method of claim 42, wherein said first opening in said substrate is formed using a process comprising mechanical drilling before said joining said first side of said first die and said substrate.

153. (previously presented) The method of claim 43, wherein said overlying metal layer comprises copper.

154. (previously presented) The method of claim 43, wherein said overlying metal layer comprises nickel.

Claim 155 (canceled)

156. (previously presented) The method of claim 52, wherein said UBM layer comprises nickel.

Claim 157 (canceled)

158. (previously presented) The method of claim 52, wherein said substrate has a thickness between 150 and 300 micrometers.

159. (previously presented) The method of claim 52, wherein said opening in said substrate is formed using a process comprising laser drilling before said joining said die and said substrate.

160. (previously presented) The method of claim 52, wherein said opening in said substrate is formed using a process comprising mechanical drilling before said joining said die and said substrate.

161. (previously presented) The method of claim 52, wherein said substrate comprises bismaleimide triazine (BT).

162. (previously presented) The method of claim 63, wherein said overlying metal layer comprises copper.

163. (previously presented) The method of claim 63, wherein said overlying metal layer comprises nickel.

Claim 164 (canceled)

165. (previously presented) The method of claim 63, wherein said substrate has a thickness between 150 and 300 micrometers.

166. (previously presented) The method of claim 63, wherein said opening in said substrate is formed using a process comprising laser drilling before said joining said die and said substrate.

167. (previously presented) The method of claim 63, wherein said opening in said substrate is formed using a process comprising mechanical drilling before said joining said die and said substrate.

168. (previously presented) The method of claim 63, wherein said substrate comprises bismaleimide triazine (BT).

169. (previously presented) The method of claim 102, wherein said UBM layer comprises nickel.

Claim 170 (canceled)

171. (previously presented) The method of claim 102, wherein said substrate has a thickness between 150 and 300 micrometers.

172. (previously presented) The method of claim 102, wherein said opening in said substrate is formed using a process comprising laser drilling before said joining said die and said substrate.

173. (previously presented) The method of claim 102, wherein said opening in said substrate is formed using a process comprising mechanical drilling before said joining said die and said substrate.

174. (previously presented) The method of claim 102, wherein said substrate comprises bismaleimide triazine (BT).

175. (previously presented) The method of claim 117, wherein said overlying metal layer comprises nickel.

Claim 176 (canceled)

177. (previously presented) The method of claim 117, wherein said substrate has a thickness between 150 and 300 micrometers.

178. (previously presented) The method of claim 117, wherein said opening in said substrate is formed using a process comprising laser drilling before said joining said die and said substrate.

179. (previously presented) The method of claim 117, wherein said opening in said substrate is formed using a process comprising mechanical drilling before said joining said die and said substrate.

180. (previously presented) The method of claim 117, wherein said substrate comprises bismaleimide triazine (BT).

181. (previously presented) The method of claim 127, wherein said substrate has a thickness between 150 and 300 micrometers.

182. (previously presented) The method of claim 127, wherein said opening in said substrate is formed using a process comprising laser drilling before said joining said first side of said die and said substrate.

183. (previously presented) The method of claim 127, wherein said opening in said substrate is formed using a process comprising mechanical drilling before said joining said first side of said die and said substrate.

184. (previously presented) The method of claim 127, wherein said substrate comprises bismaleimide triazine (BT).

185. (previously presented) The method of claim 135, wherein said overlying metal layer comprises copper.

186. (previously presented) The method of claim 135, wherein said overlying metal layer comprises nickel.

Claim 187 (canceled)

188. (previously presented) The method of claim 134, wherein said opening in said substrate is formed using a process comprising laser drilling before said joining said first side of said one of said multiple dies and said substrate.

Claims 189-194 (canceled)

195. (previously presented) A method of fabricating a chip package comprising the steps of:

providing a die, separated from a wafer, comprising a semiconductor substrate, multiple integrated circuit devices on said semiconductor substrate, multiple pads, multi-level underlying metal layers under said multiple pads, multiple insulating dielectric layers intervening said multi-level underlying metal layers, a passivation layer and an overlying metal layer, wherein said multiple pads are connected to said multiple integrated circuit devices through said multi-level underlying metal layers, wherein multiple openings in said passivation layer are over said multiple pads and expose said multiple pads, and wherein said overlying metal layer is over said passivation layer;

joining said die and a substrate, wherein an opening in said substrate exposes said overlying metal layer; and

forming a metal conductor through said opening in said substrate, wherein said metal conductor is used to connect said die to an external circuitry.

196. (previously presented) The method of claim 195, after said joining said die and said substrate, further comprising encapsulating said die with a molding material.

197. (previously presented) A method of fabricating a chip package comprising the steps of:

providing a die, separated from a wafer, comprising a semiconductor substrate, multiple integrated circuit devices on said semiconductor substrate, multiple pads, multi-level underlying

metal layers under said multiple pads, multiple insulating dielectric layers intervening said multi-level underlying metal layers, a passivation layer and an overlying metal layer, wherein said multiple pads are connected to said multiple integrated circuit devices through said multi-level underlying metal layers, wherein multiple openings in said passivation layer are over said multiple pads and expose said multiple pads, wherein said overlying metal layer is on said multiple pads exposed by said multiple openings in said passivation layer, and wherein said overlying metal layer comprises nickel;

depositing an adhesive material on a substrate;

after said depositing said adhesive material, joining said die and said substrate using said adhesive material, wherein an opening in said substrate exposes said overlying metal layer; and

after said joining said die and said substrate, forming a metal conductor through said opening in said substrate.

198. (previously presented) The method of claim 197, wherein said opening in said substrate is formed before said joining said die and said substrate.

199. (previously presented) The method of claim 197, wherein said substrate comprises bismaleimide triazine (BT).

200. (previously presented) The method of claim 197, after said forming said metal conductor through said opening in said substrate, further comprising separating said substrate into multiple portions.

Claim 201 (canceled)

202. (previously presented) The method of claim 197, after said joining said die and said substrate, further comprising encapsulating said die with a molding material.

Claims 203-208 (canceled)

209. (previously presented) A method of fabricating a chip package comprising the steps of:

providing a die, separated from a wafer, comprising a semiconductor substrate, multiple integrated circuit devices on said semiconductor substrate, multiple pads, multi-level underlying metal layers under said multiple pads, multiple insulating dielectric layers intervening said multi-level underlying metal layers, a passivation layer and a UBM layer, wherein said multiple pads are connected to said multiple integrated circuit devices through said multi-level underlying metal layers, wherein multiple openings in said passivation layer are over said multiple pads and expose said multiple pads, and wherein said UBM layer is on said multiple pads exposed by said multiple openings in said passivation layer;

joining said die and a substrate, wherein an opening in said substrate exposes said UBM layer;

after said joining said die and said substrate, depositing a conductive material into said opening in said substrate, wherein said conductive material is used to connect said die to an external circuitry; and

after said depositing said conductive material, separating said substrate into multiple portions.

210. (previously presented) The method of claim 209, wherein said UBM layer comprises copper.

211. (previously presented) The method of claim 209, wherein said UBM layer comprises nickel.

Claim 212 (canceled)

213. (previously presented) The method of claim 209, after said joining said die and said substrate, further comprising encapsulating said die with a molding material.

214. (previously presented) The method of claim 42, wherein said depositing said adhesive material on said substrate comprises printing.

215. (previously presented) The method of claim 42, wherein said adhesive material has a thickness between 10 and 100 micrometers.

216. (previously presented) The method of claim 42, wherein said adhesive material comprises polyimide.

217. (previously presented) The method of claim 42, wherein said adhesive material comprises a thermocompression material.

218. (previously presented) The method of claim 42, wherein said molding material comprises resin.

219. (previously presented) The method of claim 42, wherein said molding material comprises epoxy.

220. (previously presented) The method of claim 42, after said encapsulating said second side and sidewall of said first die, said second side and sidewall of said second die, and said gap between said first and second dies with said molding material, further comprising forming a tin-containing ball connected to said first die through said first opening in said substrate, wherein said tin-containing ball comprises a tin-lead alloy.

221. (previously presented) The method of claim 127, wherein said depositing said adhesive material on said substrate comprises printing.

222. (previously presented) The method of claim 127, wherein said adhesive material has a thickness between 10 and 100 micrometers.

223. (previously presented) The method of claim 127, wherein said adhesive material comprises polyimide.

224. (previously presented) The method of claim 127, wherein said adhesive material comprises a thermocompression material.

225. (previously presented) The method of claim 127, wherein said molding material comprises resin.

226. (previously presented) The method of claim 127, wherein said molding material comprises epoxy.

227. (previously presented) The method of claim 127, after said encapsulating said second side and sidewall of said die with said molding material, further comprising forming a tin-containing ball connected to said die through said opening in said substrate, wherein said tin-containing ball comprises a tin-silver alloy.

228. (previously presented) The method of claim 139, wherein said depositing said adhesive material on said substrate comprises printing.

229. (previously presented) The method of claim 139, wherein said adhesive material has a thickness between 10 and 100 micrometers.

230. (previously presented) The method of claim 139, wherein said adhesive material comprises polyimide.

231. (previously presented) The method of claim 139, wherein said adhesive material comprises a thermocompression material.

232. (previously presented) The method of claim 134, wherein said molding material comprises resin.

233. (previously presented) The method of claim 134, wherein said molding material comprises epoxy.

234. (previously presented) The method of claim 134, wherein said metal conductor comprises a tin-silver alloy.